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Transmission of Photovoltaic Power to Grid through Fifteen-Level Inverter

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Abstract: *In this paper, a fifteen-level inverter is developed and applied for injecting the real power of the renewable power into the grid to reduce the switching power loss, harmonic distortion and electromagnetic interference caused by the switching operation of power electronic devices. The input of the dual-buck converter is two dc capacitor voltage sources. The objective is to develop a low cost, reliable and efficient photovoltaic power supply unit for domestic applications. A fifteen level cascaded H-Bridge configuration using low voltage MOSFETs as switching devices is used. This configuration results in sinusoidal output voltages with step modulation and fundamental frequency switching. The proposed configuration will reduce conduction loss and switching loss. Simple gate drive circuit is designed using commonly available integrated circuit components. The output voltage of the dual-buck converter supplies to the full-bridge inverter. The fifteen-level output waveforms are very nearer to the pure sinusoidal output waveforms. The power electronic switches of the full-bridge inverter are switched in low frequency synchronous with the utility voltage to convert the output voltage of the dual-buck converter to a fifteen-level ac voltage. The output current of the fifteen-level inverter is controlled to generate a sinusoidal current in phase with the utility voltage to inject into the grid. The simulation is done by using MATLAB/SIMULINK software*.

Keywords: *Cascaded multilevel inverter, Developed H-bridge, Harmonic distortion, inverters, power electronics, multilevel inverter.*

I. Introduction

The full-bridge inverter is configured by two power electronic arms. The popular modulation strategies or the full-bridge inverter are bipolar modulation and uni-polar modulation. The dc bus voltage of the full-bridge inverter must be higher than the peak voltage of the output ac voltage. The output ac voltage of the full-bridge inverter is two levels if the bipolar modulation is used and three levels if the uni-polar modulation is used. The conventional single-phase inverter topologies for grid connection include half-bridge and full bridge. The half-bridge inverter is configured by one capacitor arm and one power electronic arm. The dc bus voltage of the half-bridge inverter must be higher than double of the peak voltage of the output ac voltage. The output ac voltage of the half-bridge inverter is two levels. The voltage jump of each switching is the dc bus voltage of the inverter.

Multilevel inverter can effectively reduce the voltage jump of each switching operation to reduce the switching loss and increase power efficiency. The number of power electronic switches used in the multilevel inverter is larger than that used in the conventional half-bridge and full-bridge inverters. Moreover, its control circuit is more complicated. Thus, both the performance and complexity should be considered in designing the multilevel inverter. However, interest in the multilevel inverter has been aroused due to its advantages of better power efficiency, lower switching harmonics, and a smaller filter inductor compared with the conventional half-bridge and full-bridge inverters. The voltage jump of each switching is double the dc bus voltage of the inverter if the bipolar modulation is used, and it is the dc bus voltage of the inverter if the uni-polar modulation is used. All power electronic switches operate in high switching frequency in both half-bridge and full bridge inverters.

The switching operation will result in switching loss. The loss of power electronic switch includes the switching loss and the conduction loss. The conduction loss depends on the handling power of power electronic switch. The switching loss is proportional to the switching frequency, voltage jump of each switching and the current of the power electronic switches. The power efficiency can be advanced if the switching loss of the dc–ac inverter is reduced.Two diodes are used to conduct the current loop and four power electronic switches are used to control the voltage levels. Fig. 1(a) shows the circuit configuration of the basic cascade H-bridge multilevel inverter with five-level inverter. Fig. 1(b) shows the circuit configuration of the basic cascade H-bridge multilevel inverter with fifteen-level inverter.

Multilevel inverters can synthesize higher voltages using devices of lower voltage rating. An N- level inverter output phase voltage will have N levels. The wave shape and the THD of the output voltage improve as the number of levels increase. Multilevel inverters can be used as an alternative configuration for the dc to ac inverter in photovoltaic applications. Diode clamp inverter, cascaded H-bridge inverter and flying capacitor type

inverter are the three widely used configurations of multilevel inverters [1]. Cascaded H –bridge inverter power circuit is simple and uses least number of power circuit components among these three configurations. Also cascaded H –bridge is ideally suited for systems such as photovoltaic where isolated input dc source is available

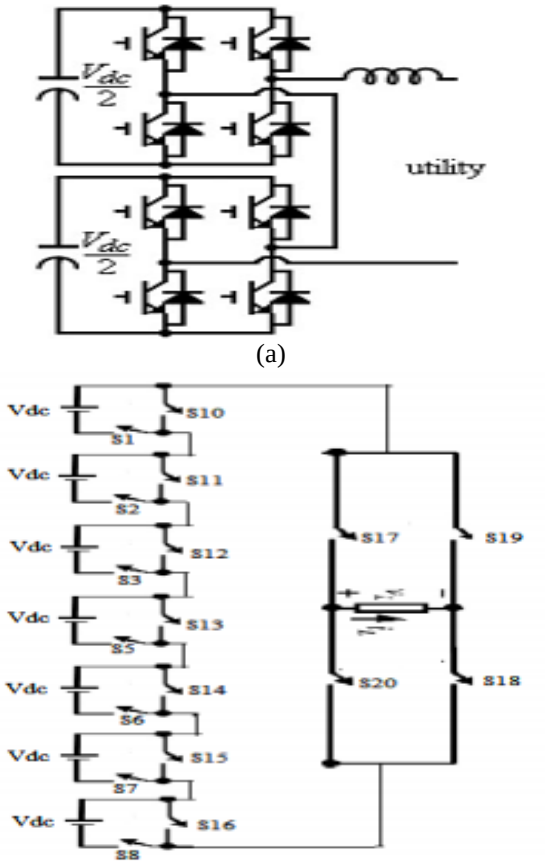

Fig.1. Circuit configuration of conventional single-phase Cascade H-bridge multilevel inverter. (a)Five-level. (b)Fifteen-level.

The fifteen-level inverter generates an output voltage with fifteen levels and applies in the output stage of the renewable power generation system to generate a sinusoidal current in phase with the utility voltage to inject into the grid. The power electronic switches of the dual-buck converter are switched in high frequency to generate a three-level voltage and balance the two input dc voltages. The power electronic switches of the full-bridge inverter are switched in low frequency synchronous with the utility to convert the output voltage of the dual-buck converter to a fifteen-level ac voltage. Therefore, the switching power loss, harmonic distortion, and electromagnetic interference (EMI) caused by the switching operation of power electronic devices can be reduced, and the control circuit is simplified. Besides, the capacity of output filter can be reduced.

Circuit diagram of a fifteen-level proposed inverter is shown in fig.1 (b). It has twenty switches and seven voltage sources. Required fifteen-level is generated by switches S1 to S16 and required polarity (fifteen-level output voltage with positive or negative polarity) is generated by switches S17 to S20. Switches S17 and S18 will produce positive half cycle output voltage and the switches S19 and S20 will produce negative half cycle output voltage.

II. Circuit Configuration

Fig. 2 shows the circuit configuration of the fifteen-level inverter applied to a photovoltaic power generation system. As can be seen, it is configured by a solar cell array, a dc–dc converter, a fifteen-level inverter, two switches and a digital signal processor (DSP)-based controller. Switches SW1 and SW2 are placed between the fifteen-level inverter and the utility andwhen islanding operation occurs, they are used to disconnect the photovoltaic power generation system from the utility. The load is placed between switches SW1 and SW2.

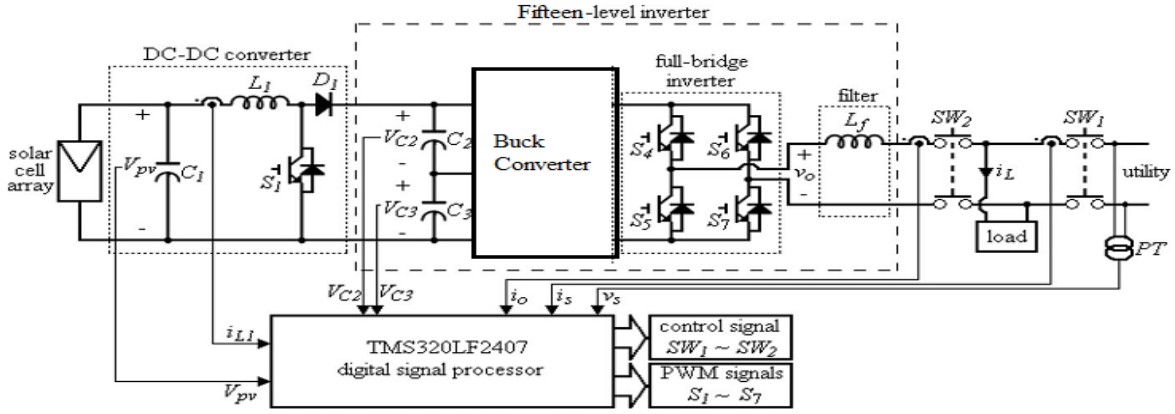

Fig.2.Circuit configuration of the developed photovoltaic power generation system.

The output of the solar cell array is connected to the input port of the dc–dc converter. The output port of the dc–dc converter is connected to the fifteen-level inverter. The dc–dc converter is a boost converter, which performs the functions of maximum power point tracking (MPPT) and boosting the output voltage of the solar cell array. This fifteen-level inverter is configured by two dc capacitors, a buck converter, a full-bridge inverter and a filter. An inductor is placed at the output of the fullbridge inverter to form as a filter inductor for filtering out thehigh-frequency switching harmonic generated by the buckconverter.

III. Operation Principle Of Cascaded H-Bridge Inverter

3.1. Working Principle

Fig.3 shows the single cell of multilevel-cascaded H-bridge configuration. The output of this cell will have three levels namely +V, 0 and –V. The switch position and the output voltage and the state of the H-Bridge are given in table I. using one single H-Bridge, a three level inverter can be realized. These H-Bridge cells can be connected in cascade to obtain multilevel-cascaded H-Bridge inverter. If V is the dc voltage of each H –bridge cell, then a five level inverter phase voltage will have five levels namely +2V, +V, 0, -V and –2V. Similarly seven level inverter will have +3V, +2V, +V, 0, -V, -2V and -3V. A five-level cascaded H-Bridge inverter requires two H-Bridges. A seven-level cascaded H-Bridge inverter requires three H-Bridges. In general N-level inverter requires (N-1)/2 H-Bridge cells in each phase and phase voltage will have N levels.

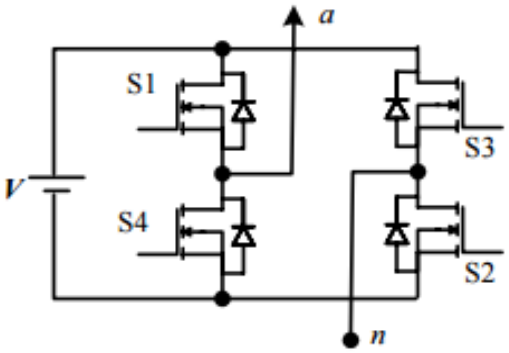

Fig.3. Power circuit of single H-Bridge cell

TABLE I: SWITCH STATUS AND STATE OF H-BRIDGE

Switch status	Output voltage (Volts)	State
S1 and S2 ON; S3 and S4 OFF	V	+1
S1 and S3 ON; S2 and S4 OFF OR S2 and S4 ON; S1 and S3 OFF	0	0
S3 and S4 ON; S1 and S2 OFF	-V	-1

3.2. Features of Cascaded H-Bridge Inverter

- Higher voltage levels can be synthesized using devices of low voltage rating. If V is the dc voltage of each of the H-Bridge cell, then each device will experience a off state voltage of V volts and a N-level cascaded H–Bridge can synthesize peak-to-peak voltage of (N*V) volts.
- Phase voltage of an N–level cascaded H-Bridge will have N levels; hence wave shape will be improved and will result in improved THD.
- Improved wave shape can be obtained even with fundamental frequency switching and step modulation. Low switching frequency will result in reduced switching loss in the devices. The switching angle of each cell can be selected to eliminate some of the lower order harmonics.
- In the above explanation, cascaded H-bridge will equal voltages are employed. However cells with different voltages can also be used. By proper selection of the voltage levels, some of the lower order harmonics can be eliminated.
- Modular structure makes the power circuit design simple and reliable. Under fault conditions, faulty cells can be bypassed and still the inverter will function with reduced output voltage levels. Since the cells are identical, faulty unit can be replaced quickly and downtime of the inverter can be reduced; hence high reliability can be achieved.
- Since the voltage across each cell is V volt, low voltage MOSFETs with high current rating can be used. Low voltage rating MOSFETs will have low$R_{DS(on)}$, so the conduction loss will be low.

3.3. Modulation Technique

The conventional photovoltaic power supply systems use two level inverters. The two level inverters employ PWM technique and generally switched at high frequency to get improved output voltage waveform. High switching frequency will result in increased switching losses in the device and also give rise to EMI problems. Compared to two-level inverter, multilevel inverter can generate near sinusoidal output voltages at fundamental frequency switching with step modulation.

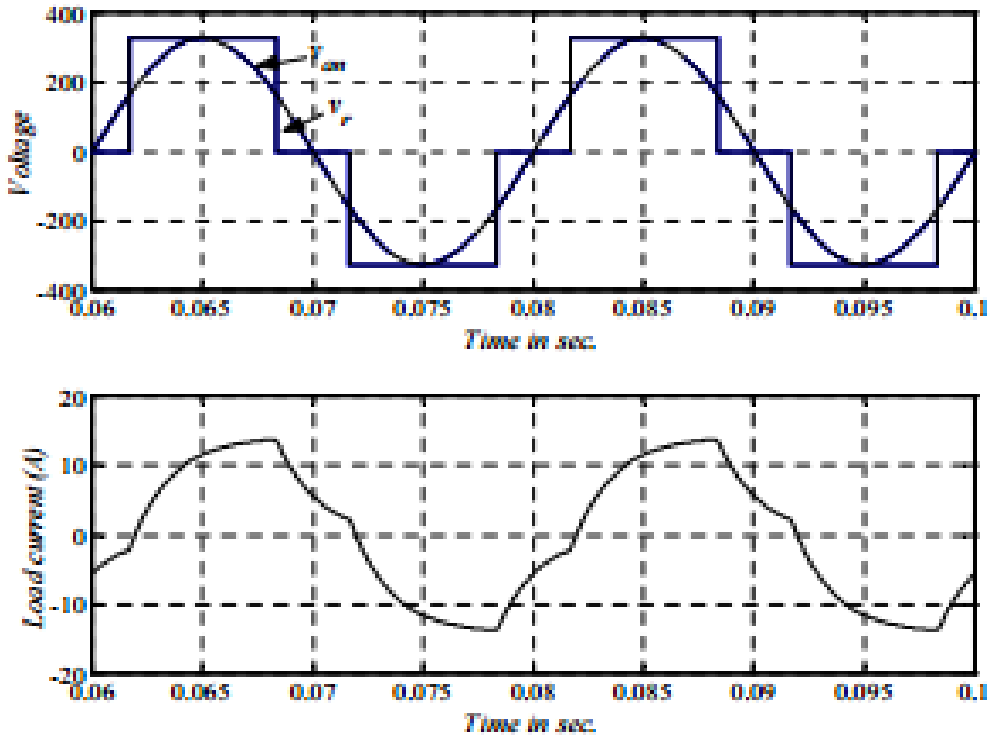

Fig.4. Output voltage and load current of the three-level cascaded H-Bridge inverter with step modulation and fundamental frequency switching

In order to study the harmonics and the THD of the output voltage and load current, multilevel inverters with N (where N is odd) varying from 3 to 21 are simulated using MATLABSIMULINK toolbox. Step modulation with fundamental frequency switching is employed. Single-phase 2KVA R-L load with 0.8 power factor is assumed. The output waveforms of three-level is shown in fig. 4.

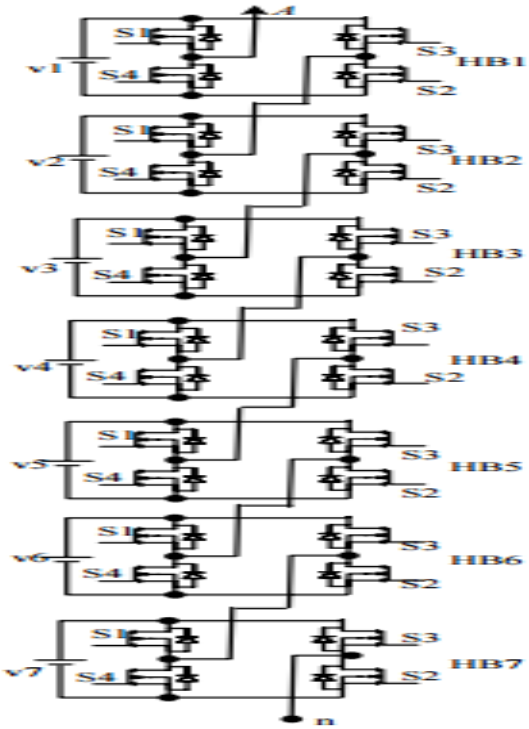

Fig.5. Power Circuit of fifteen level cascaded H –bridge inverter

Taking into consideration the voltage levels of the photovoltaic cell and the storage batteries of the proposed system, a fifteen level-cascaded H-Bridge inverter is proposed. The power circuit of the proposed fifteen level cascaded H-Bridge inverter is shown in Fig.5. The weighted THD of the phase voltage,V_{WTHD}, defined in (1), can be taken as a measure of waveform quality. In (1), V_1 is the rms value of the fundamental, h is the harmonic order and V_h is the rms value of the h^{th} harmonic component.

$$V_{WTHD} = \frac{\sqrt{\sum(V_h/h)^2}}{V_1} \qquad (1)$$

From the FFT data the$V_{WTHD}$of the phase voltage is computed using (1). It can be observed that $V_{WTHD}$is less than 0.5% for N>11.

IV. Control Block Diagram

The developed photovoltaic power generation system consists of a dc–dc power converter and the fifteen-level inverter. The dc–dc converter boosts the output voltage of the solar cell array and performs the MPPT to extract the maximum output power of the solar cell array. The controllers of both the dc–dc converter and the fifteen-level inverter are explained as follows.

4.1. Fifteen-Level Inverter

Fig. 6 shows the control block diagram of fifteen-level inverter. Besides, the fifteen-level inverter must generate a sinusoidal current in phase with the utility voltage to be injected into the utility. The subtracted result is sent to a P-I controller.

As seen in Fig. 6, the utility current is detected and sent to an RMS detection circuit. The output of the RMS detection circuit is sent to a hysteresis comparator that contains a low threshold value and a high threshold value. The output of the hysteresis comparator is sent to a signal generator. The utility voltage is detected and then sent to a phase-lock loop (PLL) circuit to generate a unity-amplitude sinusoidal signal whose phase is in phase with the utility voltage. The outputs of the multiplier and the PLL circuit are sent to the other multiplier. The output of the current-mode controller is sent to a PWM circuit to generate a PWM signal. Therefore, the fifteen-level inverter can reduce the switching loss effectively.

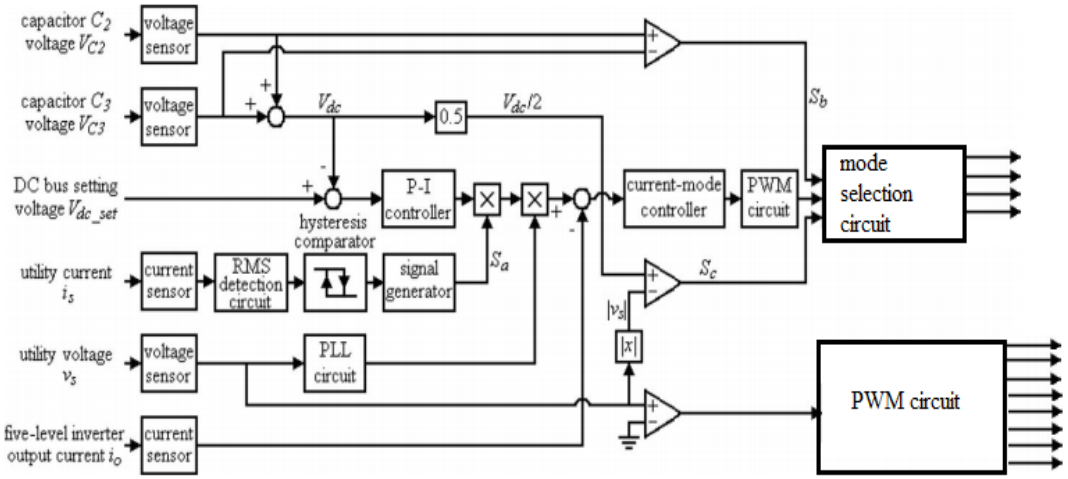

Fig.6. Control block diagram of fifteen-level inverter.

4.2. DC–DC Converter

Fig. 7 shows the control block of the dc–dc converter. The input of the dc–dc converter is the output of the solar cell array. The function of MPPT will be degraded, while the output voltage of solar cell array contains a ripple voltage. Since the output voltage of the dc–dc converter is the dc bus voltage that is controlled to be a constant voltage by the fifteen-level inverter, the outer voltage control loop is used to regulate the output voltage of the solar cell array. The perturbation and observation method is adopted to obtain the function of MPPT, and it is incorporated into the controller of the dc–dc converter. The output of the MPPT controller is the desired output voltage of the solar cell array, and it is the reference voltage of the outer voltage control loop.

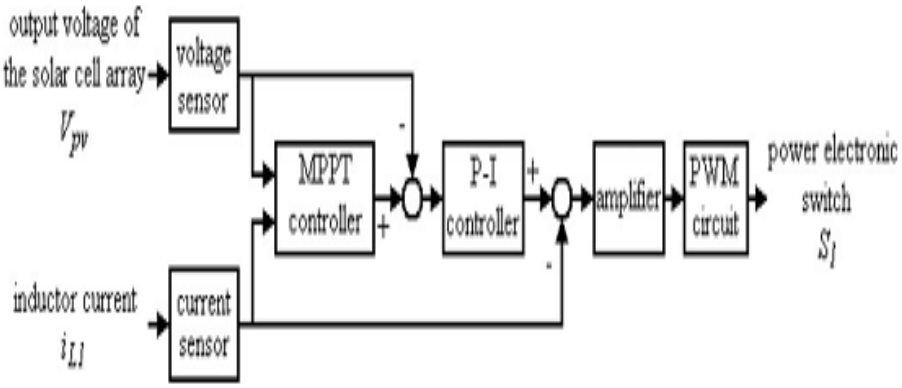

Fig.7. Control block of the dc–dc converter.

The detected output voltage and desired output voltage of the solar cell array are sent to a subtractor, and the subtracted result is sent to a P-I controller. The output of the P-I controller is the reference signal of the inner current control loop. The reference signal and the detected inductor current are sent to a subtractor, and the subtracted result is sent to an amplifier to complete the inner current control loop. The output of the amplifier is sent to the PWM circuit. The output signal of the PWM circuit is the driving signal for the power electronic switch of the dc–dc converter.

V. Simulation Results

The proposed fifteen-level inverter is simulated in MATLAB-SIMULINK toolbox. The main parameters of the simulation are listed in Table II. The solar cell array consists of two strings and each string contains eight solar modules connected in series. The capacity of solar cell array is 1.2 kW.

TABLE II: MAJOR PARAMETERS USED IN THE EXPERIMENTS

Solar module	
Rate of maximum power	75W
Open voltage	21.7V
Short current	5.0A
DC-DC converter	
Capacitor (C_1)	470μF
Inductor (L_1)	2mH
Switch frequency	20kHz
Five-level inverter	
DC bus capacitor (C_2 and C_3)	2,200μF
Filter inductor (L_f)	1.4mH
DC bus setting voltage	170V
Switch frequency (PWM)	20kHz
Utility voltage	110V
Utility frequency	60Hz

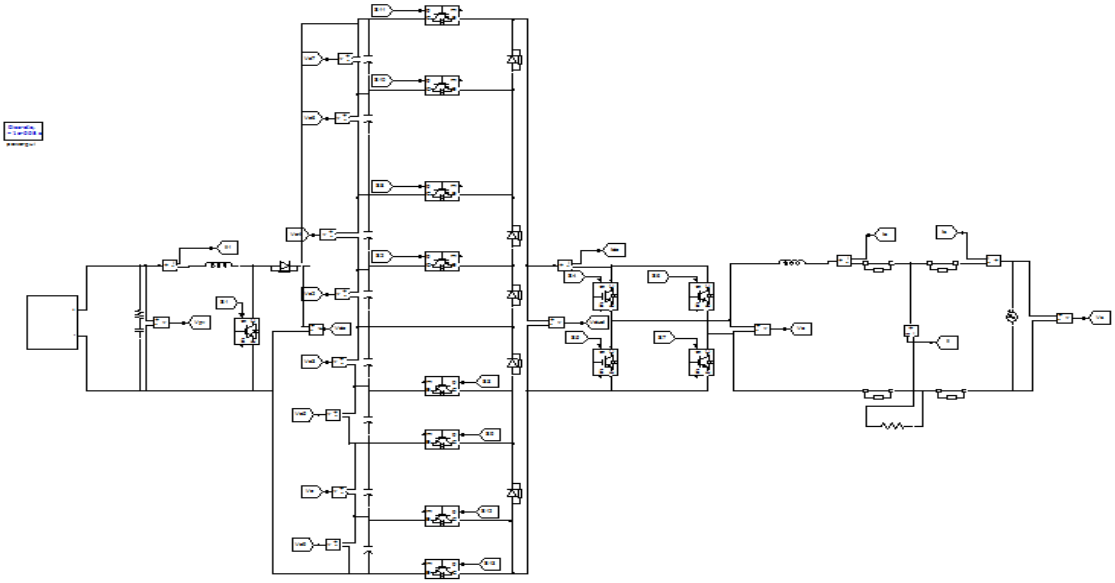

Fig.8. Matlab circuit diagram for proposed fifteen-level inverter

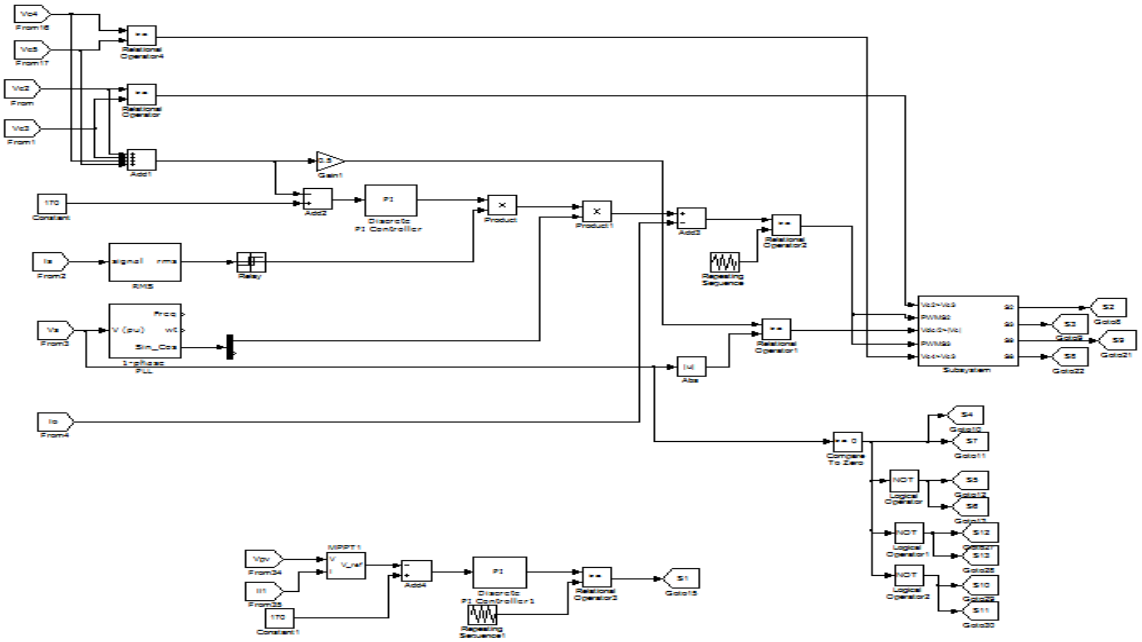

Fig.9. Matlab control circuit diagram for fifteen-level inverter and DC-DC converter

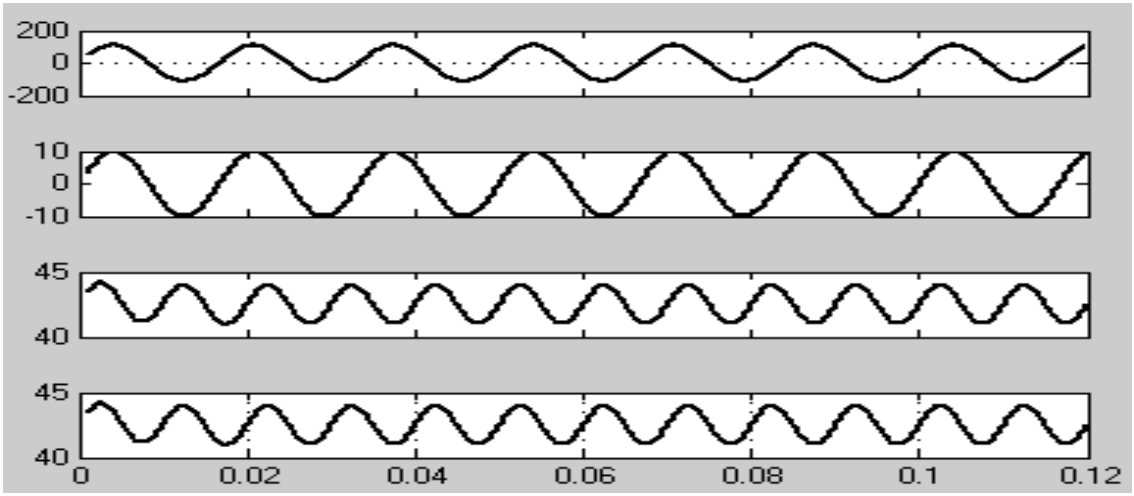

Fig.10. Simulation results of the fifteen-level inverter. (a) Utility voltage. (b) Output current of the fifteen-level inverter. (c) DC capacitor voltage VC2. (d) DC capacitor voltageVC3

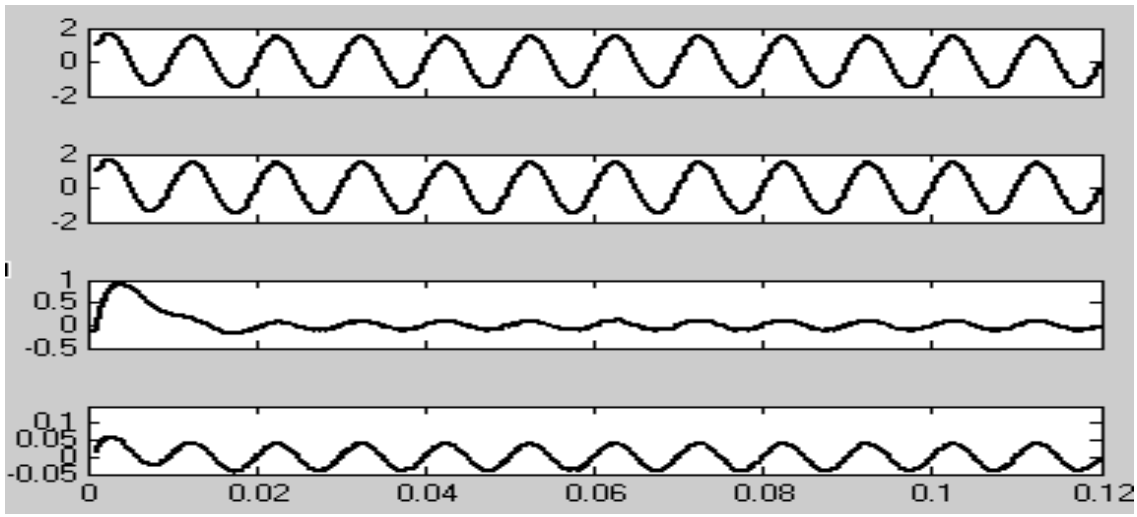

Fig.11. Simulation results for the dc–dc converter of the developed photovoltaic power generation system. (a) Voltage ripples of dc capacitor C2. (b) Voltage ripples of dc capacitor C3. (c) Output voltage ripple of solar cell array. (d) Inductor current ripple of dc–dc converter.

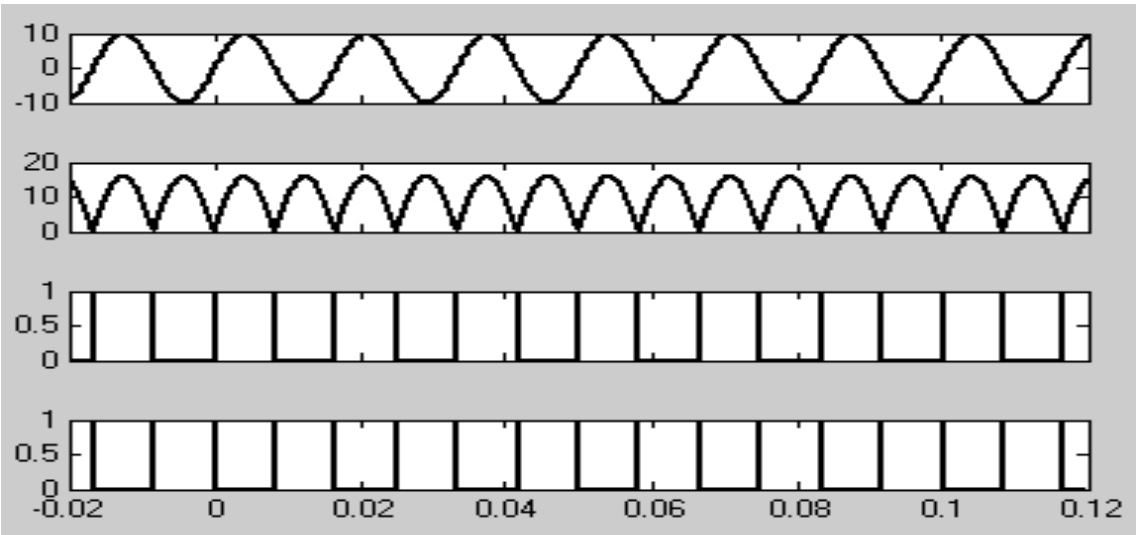

Fig.12. Simulation results for full-bridge inverter of the fifteen-level inverter. (a) Output current of the full-bridge inverter i_o. (b) Input current of the full bridge inverter i_{dc}. (c) Driver signal of S_4.(d) Driver signal ofS_5.

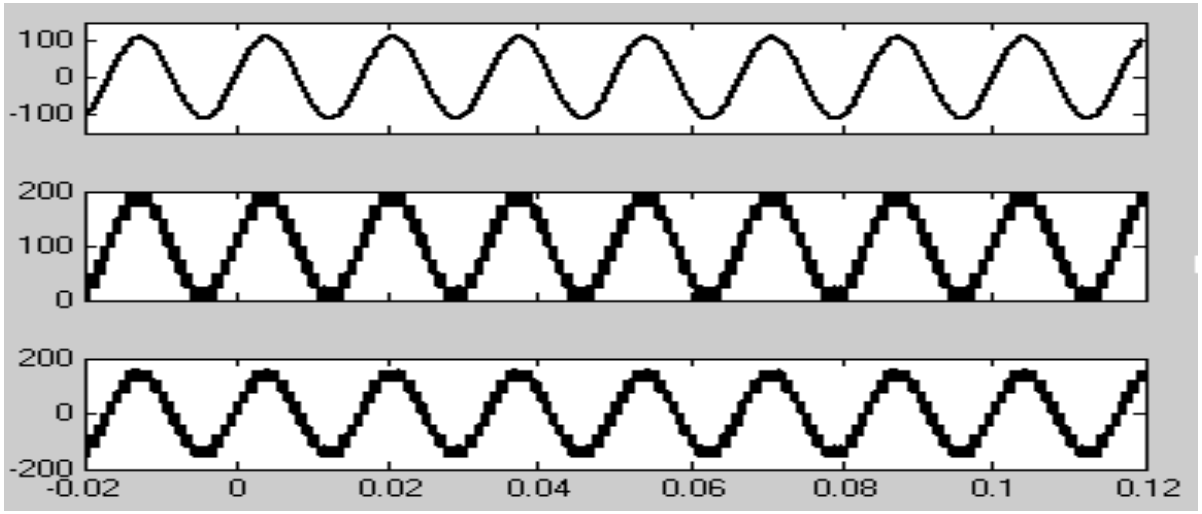

Fig.13. Simulation results of the fifteen-level inverter. (a) Utility voltage. (b) Output voltage of the full-bridge inverter. (c) Output voltage of the dual buck converter.

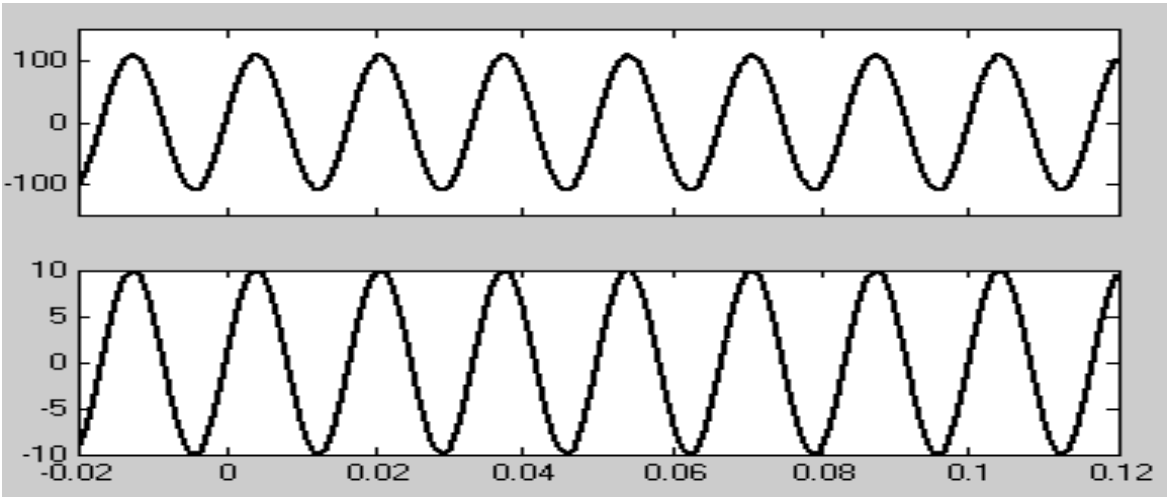

Fig.14. Simulation results for the developed photovoltaic power generation system under the distorted utility voltage. (a) Utility Voltage. (b) Output current of the fifteen-level inverter.

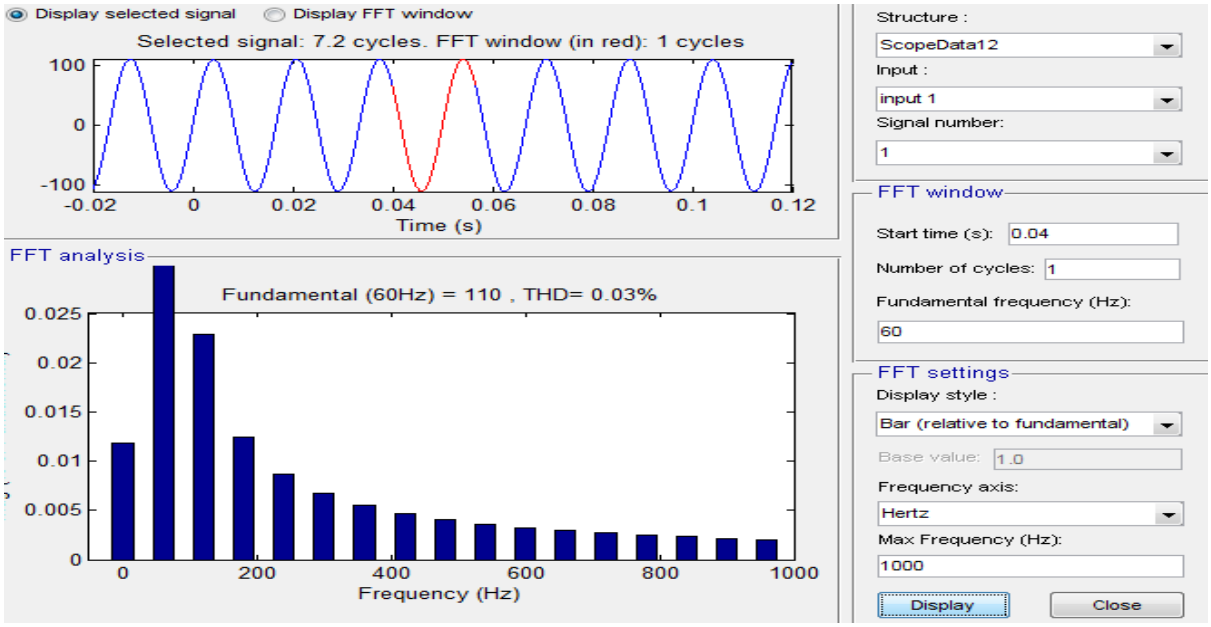

Fig.15. Harmonic spectra of utility voltage (peak value) of fifteen – level cascaded H-Bridge inverter

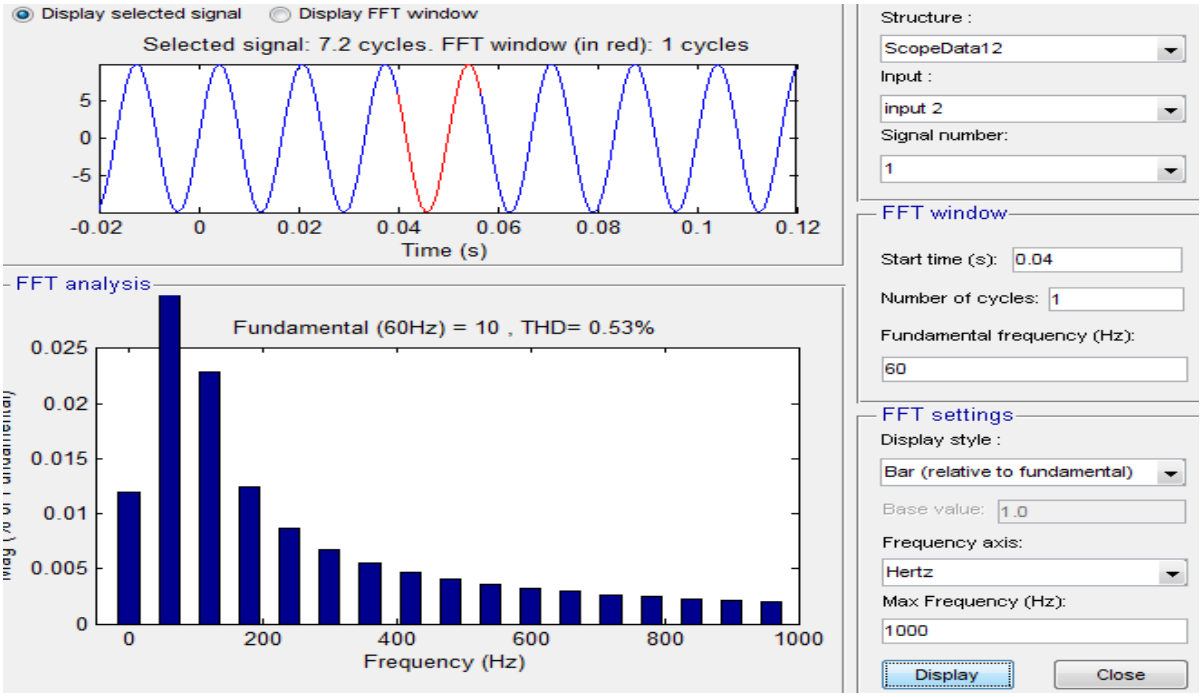

Fig.16. Harmonic spectra of output current(peak value) of fifteen – level cascaded H-Bridge inverter

Fig. 10(b) shows the output current of the nine-level inverter is sinusoidal and in phase with the utility voltage. The total harmonic distortion (THD %) of the utility voltage and the output current of the fifteen-level inverter are 0.03 and 0.53%, respectively. As seen in Fig 10(c) and 10(d), both dc capacitor voltages VC2 and VC3 remain in balance and their voltage is about 42.5V, respectively. Therefore, the dc bus voltage is regulated at 85 V. This verifies the fifteen-level inverter can perform the functions of converting solar power to ac power with unity power factor, low THD%, and balancing two dc capacitor voltages effectively. Since dc capacitors C2 and C3 perform the function of energy buffers, both dc capacitor voltages VC2 and VC3 contain a 120-Hz voltage ripple.

Fig. 11 shows the simulation results for the dc–dc converter of the developed photovoltaic power generation system. Fig. 11(a) and 11(b) show the peak-to-peak value of the voltage ripple at dc capacitors C2 and C3 are about 4V. As seen in Fig. 11(c), the peak-to-peak value of the voltage ripple at the solar cell array is only about 1.6 V. Fig. 11(d) shows the ripple of the inductor current is very small due to the use of the current mode control. In this way, the output voltage of the solar cell array can be more stable.

This verifies that the developed control method for the dc–dc converter of the developed photovoltaic power generation system can effectively block the voltage ripple of fifteen -level inverter delivering to the output voltage of the solar cell array. Fig. 12 shows the simulation results for the full-bridge inverter of the fifteen-level inverter. As can be seen, the input current i_{dc} of the full-bridge inverter shown in Fig. 12(b) is the absolute of the output current of the full-bridge inverter shown in Fig. 12(a). As seen in Fig. 12(c)and 12(d), the switch frequency of the power electronic switches S10 and S11 is 60 Hz. This verifies the power electronic switches of the full-bridge inverter are switched in low frequency, and the full-bridge inverter can convert the dc power into ac power by commutating.

Fig. 13 shows the simulation voltage of the fifteen -level inverter. As seen in Fig. 13(c), the dual-buck converter outputs a DC voltage with nine levels 4Vdc, 3Vdc, 2Vdc, Vdc, 0, -Vdc, -2Vdc, -3Vdc and -4Vdc Fig. 13(b) shows the output voltage of the buck converter is further converted to an ac voltage with fifteen voltage levels 7Vdc, 6Vdc, 5Vdc, 4Vdc, 3Vdc, 2Vdc, Vdc, 0, -Vdc, -2Vdc, -3Vdc, -4Vdc, -5Vdc, -6Vdc, and -7Vdc by the full-bridge inverter. The voltage variation of each level is Vdc. This verified that the fifteen -level inverter can generate a fifteen-level output ac voltage according to the utility voltage and only the power electronic switches of the buck Converter is switched in high frequency. Fig. 13 shows the simulation results for the developed photovoltaic power generation system under the distorted utility voltage.

As seen in Fig.14 (a), the utility voltage is distorted, .As seen in Fig. 14(b), the output current of the five-level inverter is still close to sinusoidal, and its THD% is only 053% and the power factor is 0.99. This project verifies the five-level inverter can control the output current with low THD% even when the utility voltage is distorted.As seen in Fig.15 THD% of utility voltage is 0.03% and in Fig.16 output current THD% of fifteen-level inverter is 0.53%. By using fifteen-level inverter for conversion of power, THD% of output current and utility voltage decreases.

VI. Conclusion

A fifteen-level cascaded H-Bridge based power supply unit is proposed. The simulation results are presented. A photovoltaic power generation system with a fifteen-level inverter is developed in this paper. The fifteen-level inverter can perform the functions of regulating the dc bus voltage, converting solar power to ac power with sinusoidal current and in phase with the utility voltage, balancing the two dc capacitor voltages, and detecting islanding operation. Output voltage has fifteen-level and the wave shape is near sinusoidal. The simulation results verify the developed photovoltaic power generation system, and the fifteen-level inverter achieves the expected performance. Modular structure will help in duplicating each unit. Hence for higher power rating a three phase cascaded H-Bridge can be realized. The total harmonic distortion (THD %) of the utility voltage and the output current of the five-level inverter are 4.1% and 3.3%, respectively. But, the total harmonic distortion (THD %) of the utility voltage and the output current of the fifteen-level inverter are 0.03% and 0.53%, respectively.

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